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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,452	09/26/2001	Andrew Marshall	TI-28975	5345

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EXAMINER
TANG, MINH NHUT

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,452	MARSHALL ET AL.	
	Examiner	Art Unit	
	Minh N. Tang	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 9/26/2001 (Paper No. 2) is considered by the examiner.

Specification

2. The Preliminary Amendment, claiming the benefit of 35 USC 119(e), (Paper No. 3) has been entered.

3. The disclosure is objected to because of the following informalities: on page 5, line 18, ";" should be -- . --.

Appropriate correction is required.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet ***within the range of 50 to 150 words***. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claim 12 is objected to because of the following informalities:

a/ the term "said paid" (line 4) should be -- said pad --.

b/ it appears that the preamble is inconsistent with the body of the claim, i.e. the preamble recited "method for testing integrated circuits" whereas the body of the claim recited "measuring the electrical characteristics of the selected one of said multiple test structures" and does not contain any recitation(s) for testing integrated circuits.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1-4, and 7-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 7, and 9, the limitation "the voltage" (claim 1, line 4; claim 7, lines 2-3; claim 9, line 9) has not been recited previously; therefore this term is indefinite. For examination purposes, "the voltage" is interpreted as -- a voltage --.

In claims 4, 8, and 11, the limitation "the sequence of voltages" (all in lines 2-3) has not been recited previously; therefore this term is indefinite. For examination purposes, "the sequence of voltages" is interpreted as -- sequence of voltages --.

Claims 2-3, and 10 are rejected since they depend on rejected base claims.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (U.S.P. 5,838,163).

As to claim 1, Rostoker et al. disclose, in Fig. 4b, a partially fabricated wafer, comprising: at least one probe pad (440a, 440b, and bonding pads connected to control signals 445); multiple test structures (452a, 452b, 420a-420h) which are selectably multiplexed (see column 10, lines 64-67, column 12, lines 36-39) to said probe pad (440a, 440b) in dependence on a voltage applied thereto (see column 12, lines 45-55).

As to claim 2, Rostoker et al. show in Fig. 4b, said probe pad (440a, 440b, and bonding pads connected to control signals 445) is located in a scribeline (see column 11, lines 2-6 and lines 13-15), and occupies (see the distance from pads 440a to bonding pads connected to signals 445) more than half the width of said scribeline.

As to claim 3, Rostoker et al. disclose in column 12, lines 45-55, said multiple test structures (452a, 452b, 420a-420h) are selectively multiplexed to said probe pad (440a, 440b, and bonding pads connected to control signals 445) in dependence on the voltage applied to said probe pad (440a, 440b, and bonding pads connected to control signals 445).

As to claim 4, Rostoker et al. disclose in column 12, lines 45-55, said multiple test structures (452a, 452b, 420a-420h) are selectively multiplexed to said probe pad (440a, 440b, and bonding pads connected to control signals 445) in dependence on sequence of voltages (i.e. power V+, ground V-, control signals 445, see column 12,

lines 24-31) applied to said probe pad (440a, 440b, and bonding pads connected to control signals 445).

As to claim 5, Rostoker et al. disclose, in Fig. 4b, a partially fabricated wafer, comprising: at least one probe pad (440a, 440b, and bonding pads connected to control signals 445); multiple test structures (452a, 452b, 420a-420h) which are all physically close to said probe pad (440a, 440b, and bonding pads connected to control signals 445), and which are selectably multiplexed (see column 10, lines 64-67, column 12, lines 36-39) to said probe pad (440a, 440b) in dependence on at least one global input (see column 12, lines 45-55).

As to claim 6, Rostoker et al. show in Fig. 4b, said probe pad (440a, 440b, and bonding pads connected to control signals 445) is located in a scribeline (see column 11, lines 2-6 and lines 13-15), and occupies (see the distance from pads 440a to bonding pads connected to signals 445) more than half the width of said scribeline.

As to claim 7, Rostoker et al. disclose in column 12, lines 45-55, said multiple test structures (452a, 452b, 420a-420h) are selectively multiplexed to said probe pad (440a, 440b, and bonding pads connected to control signals 445) in dependence on the voltage applied to said probe pad (440a, 440b, and bonding pads connected to control signals 445).

As to claim 8, Rostoker et al. disclose in column 12, lines 45-55, said multiple test structures (452a, 452b, 420a-420h) are selectively multiplexed to said probe pad (440a, 440b, and bonding pads connected to control signals 445) in dependence on sequence of voltages (i.e. power V+, ground V-, control signals 445, see column 12,

lines 24-31) applied to said probe pad (440a, 440b, and bonding pads connected to control signals 445).

As to claim 9, Rostoker et al. disclose, in Fig. 4b, a scribeline test circuit, comprising: a test selector circuit (452a, 452b) located in a single scribeline portion (see column 11, lines 2-6 and lines 13-15) between two adjacent die locations (102); multiple test structures (420a-420h), also located in said single scribeline portion (see column 11, lines 2-6 and lines 13-15); and at least one probe pad (440a, 440b, and bonding pads connected to control signals 445), also located in said single scribeline portion (see column 11, lines 2-6 and lines 13-15); wherein said test selector circuit (452a, 452b) makes an electrical connection from said probe pad (440a, 440b) only to a selected one (i.e. a pair of 420a, 420e in Fig. 4b) of said test structures (420a-420h), in dependence on a voltage applied at said probe pad (see column 12, lines 45-55).

As to claim 10, Rostoker et al. show in Fig. 4b, said probe pad (440a, 440b, and bonding pads connected to control signals 445) occupies (see the distance from pads 440a to bonding pads connected to signals 445) more than half the width of said scribeline.

As to claim 11, Rostoker et al. disclose in column 12, lines 45-55, said multiple test structures (420a-420h) are selectively multiplexed to said probe pad (440a, 440b) in dependence on sequence of voltages (i.e. power V+, ground V-, control signals 445, see column 12, lines 24-31) applied to said probe pad (440a, 440b, and bonding pads connected to control signals 445).

As to claim 12, Rostoker et al. disclose, in Figs. 3a and 4a, an apparatus and method for testing integrated circuits, comprising the steps of:

(a.) applying a selection signal (control signals 445) to a probe pad (bonding pads connected to control signals 445, pad 440), to drive a selector circuit (450) to connect a selected one (one of the dies 102 via 420a in Fig. 4a) of multiple test structures (dies 102) to said pad (440); and

(b.) applying a controlled voltage (see column 12, lines 10-15) to said pad (440), and thereby measuring the electrical characteristics (i.e. burn-in, or cross-check testing) of the selected one (one of the die 102) of said multiple test structures (dies 102).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Tsuji et al.	6,291,835	Semiconductor Device.
Pappert et al.	5,929,650	Method And Apparatus For Performing Operative Testing On An Integrated Circuit.
Goto	5,446,395	Test Circuit For Large Scale Integrated Circuits On A Wafer.
Farnworth et al.	5,059,899	Semiconductor Dies And Wafers And Method For Making.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh N. Tang whose telephone number is (703) 305-1652. The examiner can normally be reached on M-F (6:30-4:00) first Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mrs. Cuneo, Kamand can be reached on (703) 308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

Minh Tang
January 24, 2003